METASAT

MODULAR MODEL-BASED DESIGN AND TESTING FOR APPLICATIONS IN SATELLITES

METASAT’s Model-Based Design Solutions

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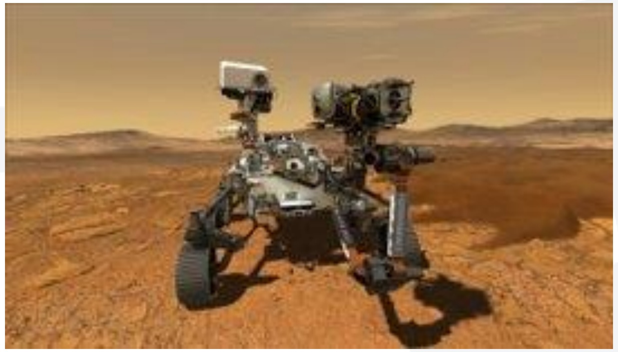
16/06/2023

Introduction

- Modern and upcoming space systems require increasing levels of computing power
- Traditional space processors cannot provide this performance level
- Need for higher performance hardware in space systems



METASAT Overview

- Modern aerospace systems require new, advanced functionalities
  - Artificial Intelligence (AI)
  - High Resolution Sensors
  - Optical communications
  - Advanced Robotics…
- Advanced functionalities require complex hardware and software compared to the existing space technologies
- High Performance Hardware technologies: Advanced Multi-cores, GPUs, AI accelerators
- Programming high performance hardware requires complex software: parallel and GPU programming

Model-Based Design

- Model-Based Design can reduce the development and verification time for these complex platforms
- Development can be assisted by high level design methods (models) from which code can be automatically generated
  - Correct-by-construction
  - Various levels of verification: model-in-the-loop, software-in-the-loop, processor-in-the-loop etc
  - Virtual platforms allow starting software development before the hardware is ready
  - Break the dependency between hardware and software development

Virtualisation

- Time and Space isolation provide benefits for faster and easier integration
- Components can be developed and tested in isolation
- Fault Detection, Isolation and Recovery (FDIR)

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- 2-year Horizon Europe project: January 2023-December 2024
- TRL 3-4

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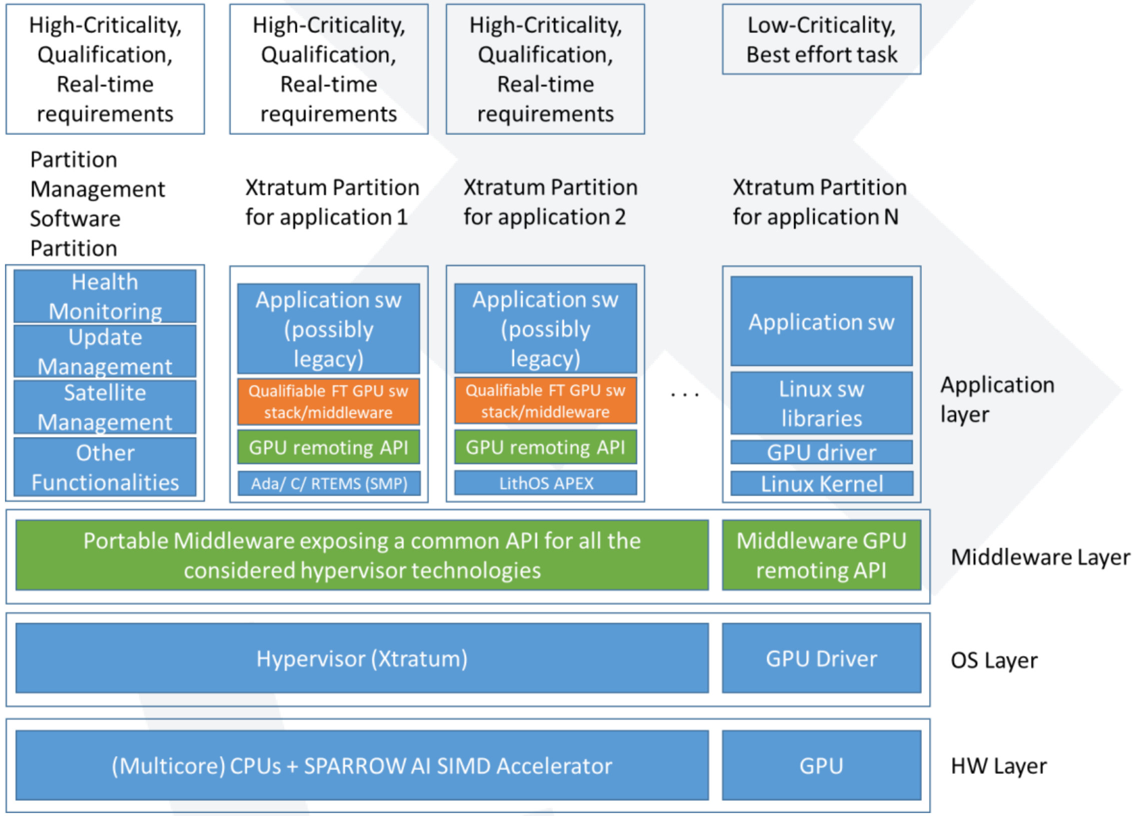
- METASAT will rely on open source and standardized technologies
  - Maximise interoperability and avoid vendor lock-in
  - Facilitate the development of a space ecosystem
- ESA's TASTE Open Source Model Based Design framework, enhanced with code generation for high performance platforms such as GPUs
- Open Source Processor technologies such as NOEL-V RISC-V processors
  - Enhancement with AI processing acceleration capabilities
- Virtualisation support for GPUs and AI acceleration capabilities
  - Novel AI approaches for integration testing and FDIR

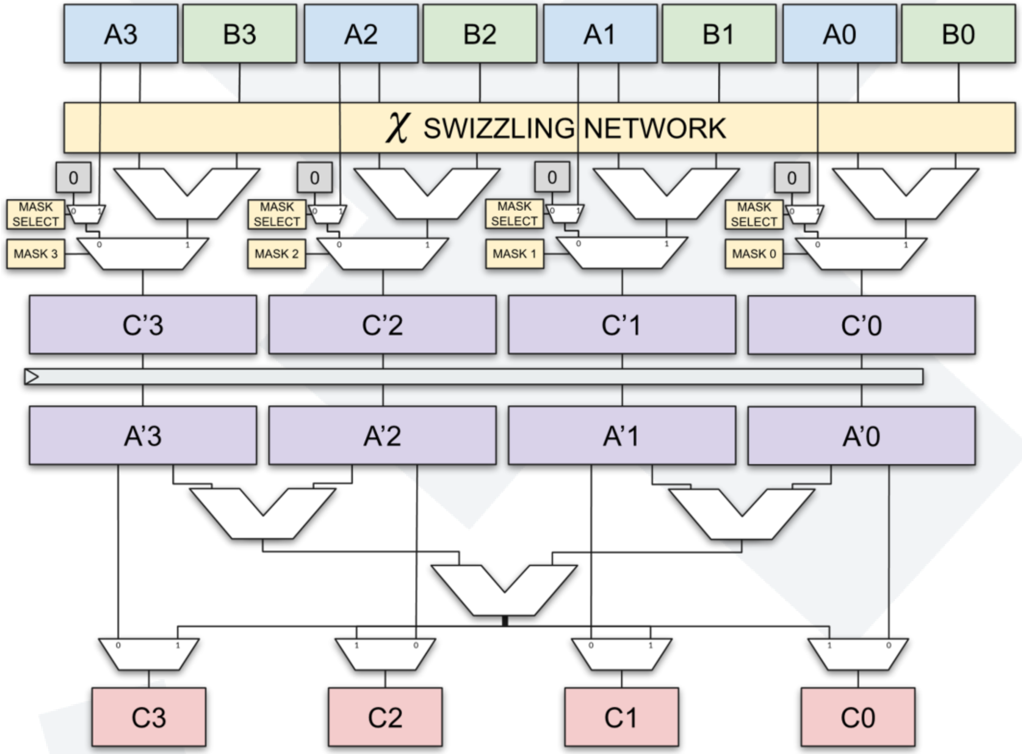
The METASAT RISC-V Platform

- Mixed Criticality Platform
- FPGA Prototype on a Xilinx VCU118
- Multicore CPU Based on NOEL-V + SPARROW AI SIMD Accelerator
  - Qualifiable software stack for high criticality software with moderate AI acceleration needs



The METASAT RISC-V Platform

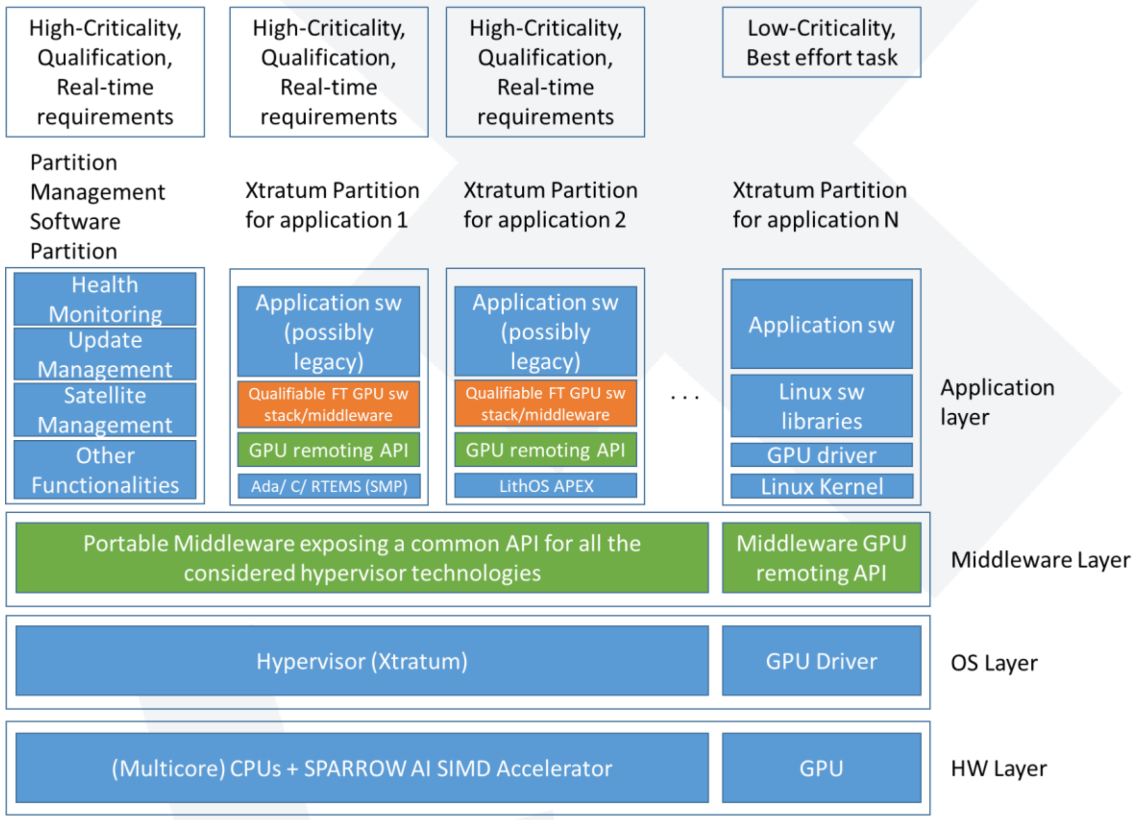
- SPARROW AI SIMD Accelerator [1]
- High-performance, Low-cost at least 30% smaller than conventional vector processors with similar performance
- Minimal core modifications
  - incremental qualification
- Key features: reuse of integer register file, short SIMD unit (8-bit), swizzling, reductions
- Intrinsics-like software support similar to ARM's NEON



[1] M. Solé, SPARROW: A Low-Cost Hardware/Software Co-designed SIMD Microarchitecture for AI Operations in Space Processors, DATE 2021

The METASAT RISC-V Platform

- Mixed Criticality Platform
- FPGA Prototype on a Xilinx VCU 118
- Configurable Vortex RISC-V GPU [1]
  - Enhancements for real-time execution and reliability
  - Qualifiable software stack for tasks requiring very high performance
  - Enable the use of GPUs from bare metal, or RTOS
  - Share the GPU among partitions
- The hardware platform will be open sourced as well as much of its software



[1] B. Tine et al, Vortex: Extending the RISC-V ISA for GPGPU and 3D-Graphics, MICRO 2021

The METASAT RISC-V Platform

- Mixed Criticality Platform
- FPGA Prototype on a Xilinx VCU 118
- Ethernet connectivity through Gaisler's GRLIB Ethernet controller (greth)
- Currently the driver is getting ported to Xtratum

```
greth0      Cobham Gaisler  GR Ethernet MAC
            AHB Master 4
            APB: fc084000 - fc084100
            IRQ: 5
            edcl ip 192.168.125.2, buffer 16 kbyte
```

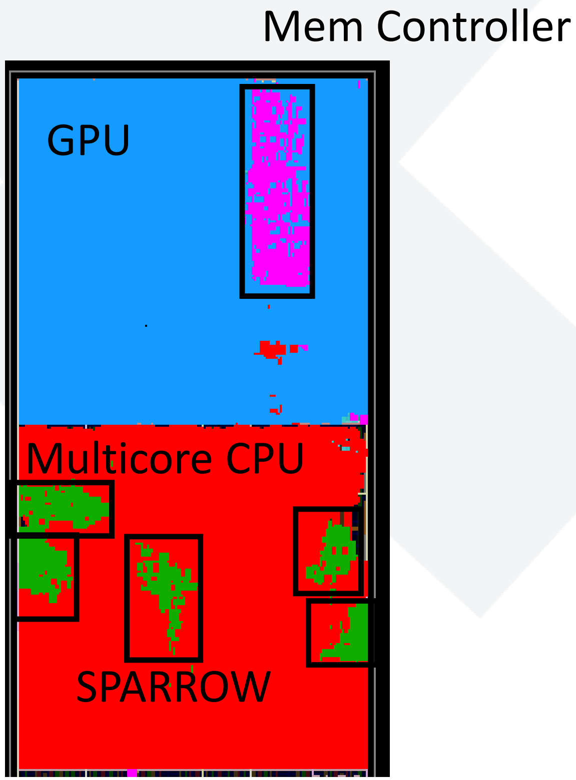
```
# ssh msole@192.168.125.1
The authenticity of host '192.168.125.1 (192.168.125.1)' can't be established.
ED25519 key fingerprint is SHA256:W6uPqsqLxV6etVMjbRiW7rcC/9QVKjl5BjlNcrfVBak.
This key is not known by any other names
Are you sure you want to continue connecting (yes/no/[fingerprint])? yes
Warning: Permanently added '192.168.125.1' (ED25519) to the list of known hosts.
msole@192.168.125.1's password:
Welcome to Ubuntu 18.04.6 LTS (GNU/Linux 4.15.0-208-generic x86_64)

 * Documentation:  https://help.ubuntu.com
 * Management:     https://landscape.canonical.com
 * Support:        https://ubuntu.com/advantage

90 updates can be applied immediately.
To see these additional updates run: apt list --upgradable

Ubuntu comes with ABSOLUTELY NO WARRANTY, to the extent permitted by
applicable law.

New release '20.04.6 LTS' available.
Run 'do-release-upgrade' to upgrade to it.

*** /dev/mapper/vg_docker-lv_docker will be checked for errors at next reboot ***
*** /dev/sdc1 will be checked for errors at next reboot ***
*** /dev/sda2 should be checked for errors ***

*** System restart required ***
Last login: Tue May  2 11:56:43 2023 from 84.88.51.129
msole@Caos17:~$ ls
bin        GitHub.token   OBPMark               sim
bitstream  grlib-sparrow  opt                   test
FPGA_SW    metasat        selene-hardware-caos  tflite-micro_hello_noel-v
msole@Caos17:~$
```

The METASAT RISC-V Platform: Current Status

- NOEL-V Integration with Vortex GPU
  - AXI interface added to Vortex
  - Started a simple experiment offloading a GPU kernel to the GPU
    - Established a programming methodology for using OpenCL in the METASAT platform Precompile a GPU kernel
        - Common practice in safety critical systems (OpenGL SC, Vulkan SC)
      - Include the kernel binary in the program executable in a dedicated GPU memory area
        - No filesystem
      - Linker script modifications

The METASAT RISC-V Platform: Current Status

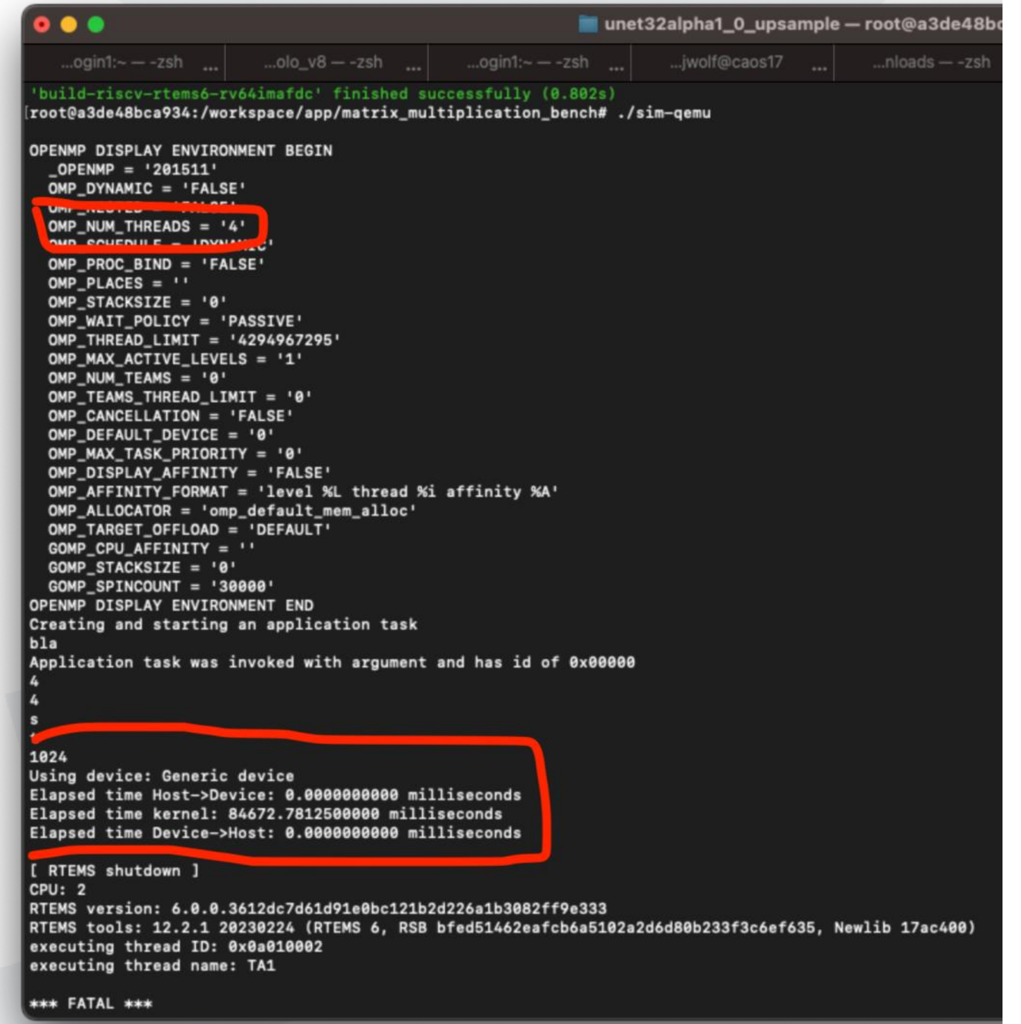
- FPGA Resource utilisation
- Current configuration:
  - 4 NOEL-V high performance + 2 SPARROW accelerators: 48% utilisation
  - To include also L2 cache L2Lite
  - GPU: 4 CUs, 4 threads each, 64bit L2 GPU cache 50% Utilisation
  - Once the design is fully functional a design space exploration will be performed to find the best configuration for the project use cases



The METASAT RISC-V Platform: Current Status

- Able to run a simple OpenMP program on both FPGA and QEMU under RTEMS

- On going work to support SPARROW in RTEMS
  - RTEMS Compiler modifications completed
  - Support for SPARROW control register to be added to RTEMS



The METASAT RISC-V Platform: Current Status

- Preliminary Results

```
Max number of threads in OpenMP using omp_get_max_threads() is 4
Block size: 1024
base 1core: 392.225896 s
transposed 1core: 86.701770 s - valid
omp 4cores: 280.271344 s - valid
omp transposed 4core: 19.934385 s - valid
sparrow 1core: 20.878695 s - expected error (non transposed sparrow)
sparrow transposed 1core: 19.400293 s - valid
sparrow omp 4core: 6.340939 s - expected error (non transposed sparrow)
sparrow omp transposed 4core: 5.664588 s - valid
```

4.4x

4.5x

15.3x

- SPARROW on a single core NOEL-V provides similar performance with a 4-core OpenMP implementation

- 15x overall speedup by using both multicore and SPARROW

The METASAT RISC-V Platform: Current Status

- Preliminary Results

```
Block size: 4096
base 1core: 29057.139986 s
transposed 1core: 5757.967587 s - valid
omp 4cores: 23248.178855 s - valid 4.3x
omp transposed 4core: 1339.930062 s - valid
sparrow 1core: 2001.829881 s - expected error (non transposed sparrow)
sparrow transposed 1core: 1452.943046 s 3.9x valid
sparrow omp 4core: 1001.405814 s - expected error (non transposed sparrow)
sparrow omp transposed 4core: 852.343338 s 6.7x valid
```

- SPARROW on a single core NOEL-V provides similar performance with a 4-core OpenMP implementation

- 6.7x overall speedup by using both multicore and SPARROW when the data doesn't fit in the L2 cache
  - Still opportunity for optimisation, e.g. to implement a cache blocking solution

The METASAT Virtual RISC-V Platform

- Multicore CPU to be modeled in QEMU
  - Add also support for SPARROW
- Vortex GPU to be simulated in Verilator
  - Cycle-accurate behavioural simulation
  - SystemVerilog to SystemC/C++

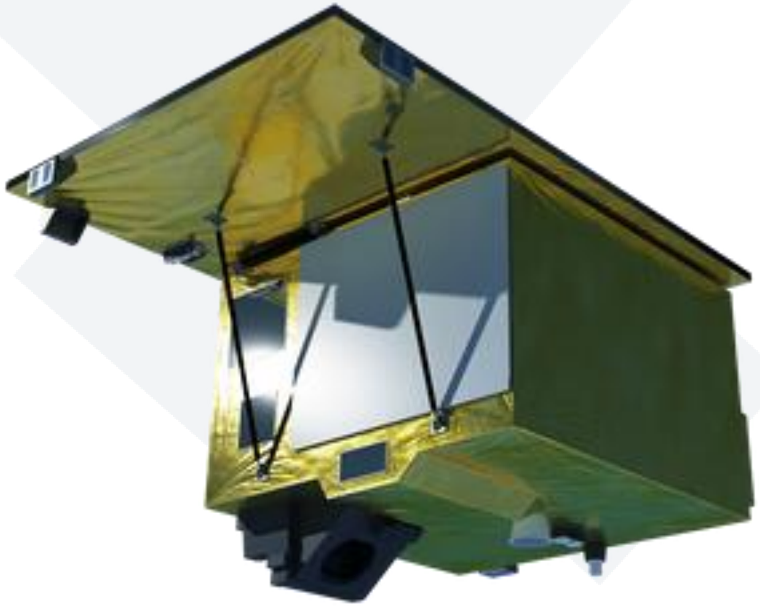
The METASAT Model-based Toolchain

- Primary focus on TASTE
  - Extend it with support for RISC-V and the METASAT platform
    - Code generation, compilation, simulation
  - Include support for SPARROW
  - Add support for Xtratum configuration for multicores
  - Shared use of devices like the Ethernet, UART and GPU
  - Integration with GPU code generated from Matlab/Simulink GPU coder
  - Configuration for OpenMP, OpenCL and other safety critical GPU languages such as Brook Auto[1], OpenGL SC 2.0, Vulkan SC, SYCL SC
  - Ada SPARK contracts for GPU code
  - Support for at least one ML framework, e.g. TensorFlow-Lite or ONNX
- All improvements will be upstreamed to TASTE's and related repositories (e.g. Ocarina)

[1] M. M. Trompouki, L. Kosmidis, Brook auto: high-level certification-friendly programming for GPU-powered automotive systems, DAC 2018

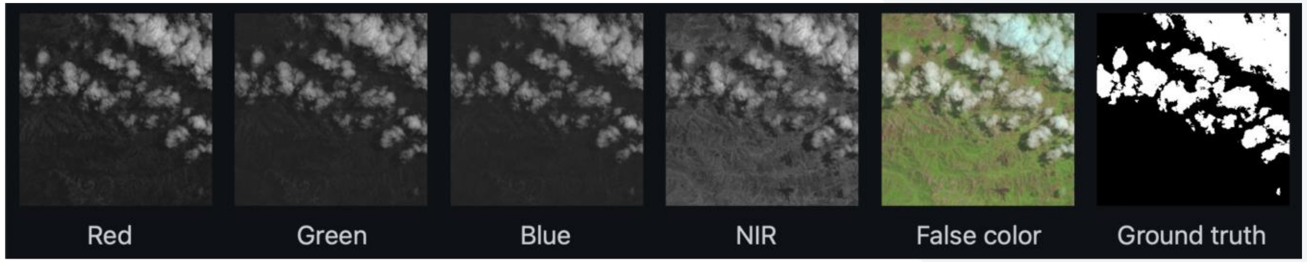
Project Use Cases

- 3 Project Use cases will be implemented
- OHB/DLR Use Case
  - Hardware interlocking
    - Protect against wrong software behaviour
  - Implement interlocks at software level instead of hardware
    - Reduce cost
  - Implement AI Based FDIR
    - To be accelerated on the CPU using the SPARROW AI accelerator
  - Housekeeping data from the ENMAP satellite



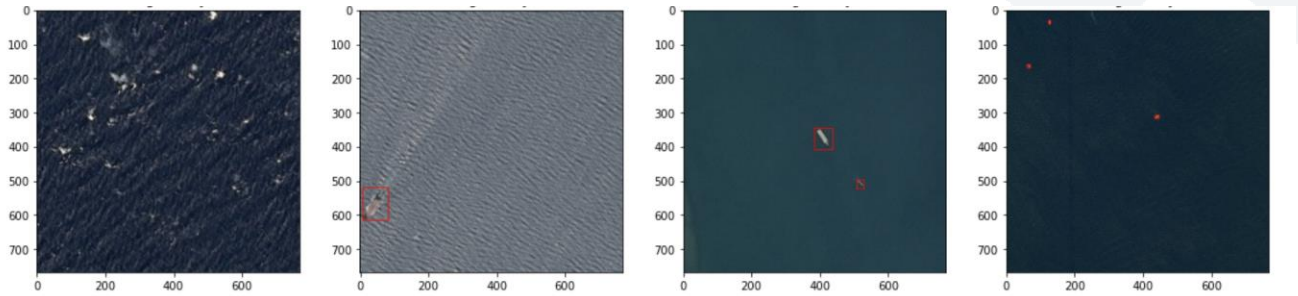
Project Use Cases

- 2 BSC-provided use cases based on OBPMark-ML [1][2]
- Cloud screening



4 Channels RGB/NIR mapped to binary mask (cloud/no cloud)

- Ship Detection



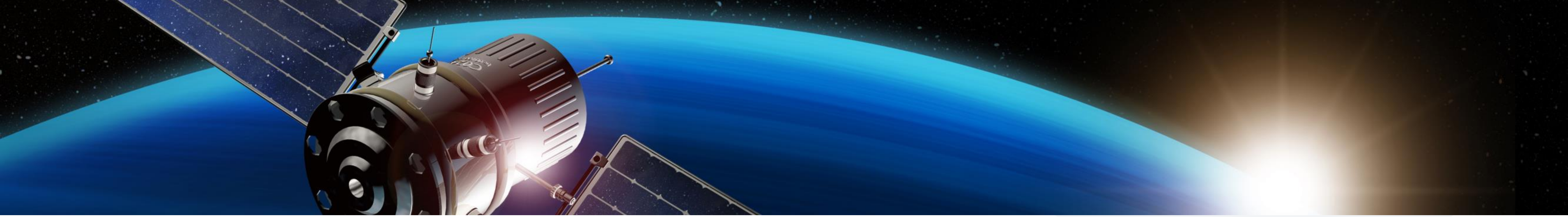
- To be executed on the GPU

[1] D. Steenari et al, OBPMark (On-Board Processing Benchmarks) – Open Source Computational Performance Benchmarks for Space Applications, European Workshop on On-Board Data Processing (OBDP2021). https://doi.org/10.5281/zenodo.5638577

[2] http://obpmark.org

Conclusion

- METASAT will achieve a major milestone towards the use of GPUs and high performance platforms in space through model based design
- Will provide an open source reference hardware platform
  - FPGA and virtual
- Solve key limitations preventing GPUs to be adopted today in institutional missions
  - Qualifiable software stack
- Improvements in model based design tools for high performance platforms
- Open source contributions



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METASAT has received funding from the European Union's Horizon Europe programme under grant agreement number 101082622.